# A FLIP CHIP BONDING TECHNOLOGY USING GOLD PILLARS FOR MILLIMETER-WAVE APPLICATIONS

**S. Aoki, H. Someta, S. Yokokawa, K. Ono, T. Hirose and Y. Ohashi**
**FUJITSU LABORATORIES LTD.**
**10-1, Morinosato-Wakamiya, Atsugi 243-01, Japan**

## ABSTRACT

This paper reports a flip chip bonding technology for a millimeter-wave monolithic integrated circuit (MIMIC) using gold micropillars with a controlled air gap instead of conventional wire bonding. We focus on their electrical performance in the W-band and their reliability against stresses expected in automotive radar applications.

## INTRODUCTION

The demand for commercial applications of millimeter-wave radio systems is increasing with advances in automotive safety and high-speed wireless communications. [1] The millimeter-wave automotive radar is expected to be a key component in improving the driving safety toward the next century.[2]

There are four factors necessary in achieving a practical automotive radar: performance, cost, reliability, and physical size. Flip chip bonding is expected to be the best solution for first level (bare chip) packaging, because of its short interconnection length. This leads to a low performance loss and size reduction, and its precision in assembly enables low cost fabrication.[3]

However, two problems remain. Firstly, there is the proximity effect from the transmission line on the chip to the substrate on the high frequency characteristics of the device. Secondly, their reliability could fall when subjected to thermal and mechanical stresses inherent in the inflexible structure of flip chip bonding. We investigated the high frequency characteristics and the reliability of the flip chip bonding portion between a gallium arsenide chip and an alumina substrate.

## EXPERIMENT

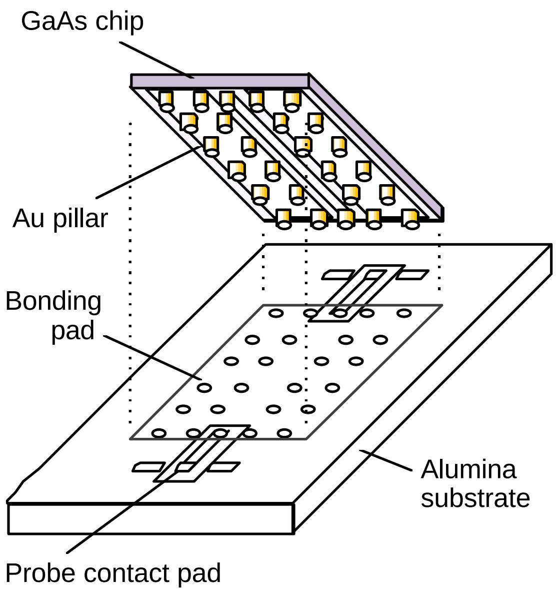


**Fig.1 Schematic diagram of the test piece with a GaAs chip flip-chip-bonded on alumina substrate using gold pillars.**

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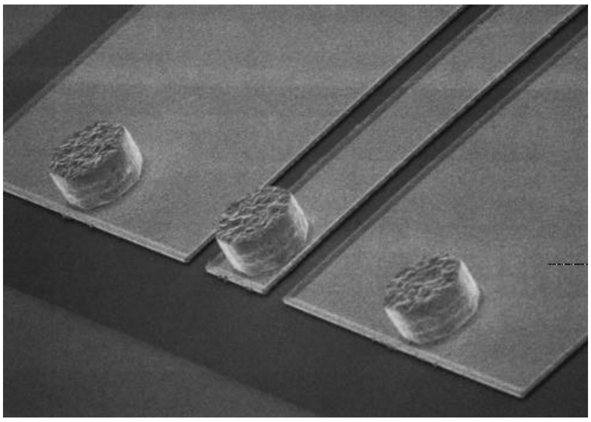

**Fig.2 Gold pillars deposited on transmission line on GaAs chip.**

In the fabricated samples, a gold-tin eutectic reaction method was employed for flip chip bonding, in which the chip and the substrate were heated after the gold pillars on the chip were connected to the tin of the substrate. This process potentially causes less damage to the fragile gallium arsenide chips than conventional gold to gold thermocompression bonding [4, 5] because of its lower temperature and lower load. In addition, using the gold-tin method avoids solder contamination of the gold transmission line on the chip, which can be a problem in solder bump bonding method.[6]

The test piece consisted of a 2-mm-square 0.25-mm-thick gallium arsenide chip with gold transmission lines and gold pillars on one surface, and a 10-mm-square 0.65-mm-thick alumina substrate with a patterned thin film metallization on it's surface. Gold pillars 40-µm in diameter and 20-µm high were deposited on the transmission line by electroplating, as shown in Figure 2. The substrate metallization consisted of 100 nm of Ti, 3,000 nm of Cu, and 500 nm of Sn. The chip was mounted on the substrate with a pulse-heat tool at 350°C for 10 seconds with a 20 g/pillar load. The test piece structure is shown in Figure 1.

The scattering parameters were measured from 0.5 to 85 GHz with a Wiltron -type 360B Vector Network Analyzer. Reliability was estimated by a thermal cycle test (in air), a thermal shock test (in liquid), and a vibration test.

## RESULTS AND DISCUSSIONS

Figure 3 shows the scattering parameters of the sample: S21 at 77 GHz measures -1.8 dB. By removing the return loss (-0.3 dB), the loss from the substrate coplanar lines (-0.5 dB) and the transmission line on the chip (-0.6 dB), the insertion loss of the pillar portion is estimated to be -0.2 dB/pillar. Figure 3 also shows that S11 is below -15 dB at 77 GHz. Typical values for wire bonding were estimated at -0.6 dB for S21, and -10 dB for S11 in simulation.[3] These results show that flip chip bonding has both a lower insertion loss and a lower return loss than conventional wire bonding.

Next, we estimated the proximity effect on the high frequency characteristics of the device, resulting from the proximity of the transmission line on the chip to the substrate. Figure 4 shows the relationship between the

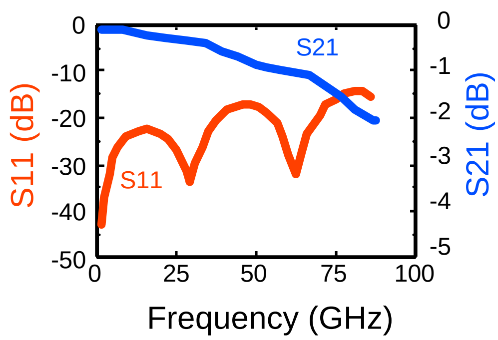


**Fig.3 Scattering parameters of the fabricated module.**

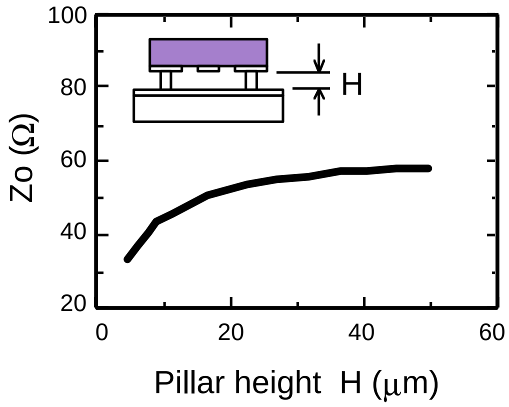


**Fig. 4 The effect of pillar height on characteristic impedance of chip coplanar line.**

characteristic impedance of the transmission line on the chip and the pillar height (in simulation). The transmission line on the chip is coplanar in structure for a 20 μm gap and 20 μm line width. The characteristic impedance gradually decreases with a decrease in the pillar height. A ± 5 μm change in the height of a 20-μm-high pillar results in a ± 2 Ω change in the 52 Ω characteristic impedance. The slope of the curve becomes remarkable below a 15 μm pillar height. This

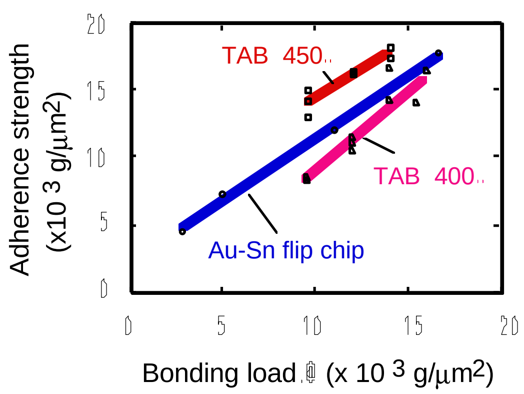


**Fig. 5 Bonding strength of Au-Sn flip chip compared to TAB bump[7)]**

is possibly explained by the change in the transmission mode. The result indicates that flip chip needs a bonding technology with a controlled air gap, especially at a low pillar height such as 10 μm. The gold-tin eutectic bonding method is attractive because of its low load in the bonding process.

Figure 5 shows the pillar adherence strength, measured by the die shear strength of the flip-chipped GaAs chips, compared with the bump shear strength of conventional tape automated bonding (TAB).[7)] The pillar adherence strength was equivalent to or larger than the TAB bump adherence strength.

In general, the major problem in flip chip bonding is the thermal expansion mismatch between a chip and substrate, because both are inflexible and thermal stress concentrates on the bonding portion. Gallium arsenide has a thermal expansion coefficient (6.0 ppm/$^{o}$C) similar to that of alumina (6.5 ppm/$^{o}$C), a typical substrate material. In addition, millimeter-wave devices are small in size reflecting the short wavelength; a typical size is 3-mm square. Accordingly, the flip chip bonding of gallium arsenide devices on an alumina substrate is expected to have a relatively small thermal expansion mismatch and, therefore, a high reliability.

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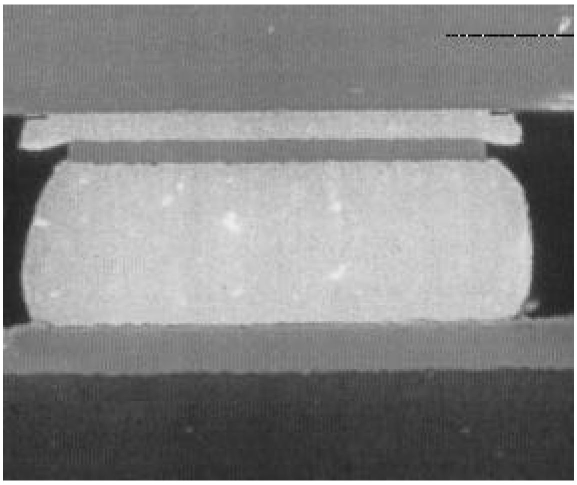

**Fig.6 SEM image of cross-section of Au-Sn flip chip bonding**

Table 1 shows the test conditions and the results of the reliability test. The sample is 3-mm square and bonded to an alumina substrate with sixteen pillars. All the samples passed the thermal cycle test, the thermal shock test and the vibration test. Figure 7 shows a cross-section of the flip chip bonding after the thermal cycle test. This data indicates that the bonding technology has a high reliability.

## CONCLUSION

We propose a new packaging design for GaAs MIMIC with a flip chip bonding technology using gold micro pillars and tin metallization on an alumina substrate. The measured scattering parameters at 77 GHz shows that pillar insertion loss is -0.2 dB and pillar return loss is below -15 dB, confirming that the flip chip bonding has a higher transmission performance than conventional wire bonding in the W-band. The investigation of the relationship between the characteristic impedance of a chip transmission line and pillar height provides a practical scale design for reducing the proximity effect between the chip transmission line and substrate. Results of reliability tests indicate that the flip chip bonding is very resistant to thermal and mechanical stresses and seems to be suitable for practical applications including automotive radars.

References;

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**Table 1 Reliability test : conditions and results.**

| Test item | Condition | Defect rate* |
|---|---|---|
| Thermal cycle (in air) | -55 to 150°C, 1000 cycles | 0/20 |
| Thermal shock (in liquid) | 0 to 100°C, 1000 cycles | 0/20 |
| Vibration | 10 to 200 Hz, 10 G, 6 hours | 0/12 |

*** Chip count base. Each chip has sixteen pillars and bonding points.**

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